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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/060,750 | 01/30/2002 | Robert J. Devins | BUR9-2001-0016-US1 | 7058 |

29154 7590 10/18/2007

FREDERICK W. GIBB, III
Gibb & Rahman, LLC
2568-A RIVA ROAD
SUITE 304
ANNAPOLIS, MD 21401

| EXAMINER | |
|---|---|
| SHARON, AYAL I | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2123 | |

| MAIL DATE | DELIVERY MODE |
|---|---|
| 10/18/2007 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/060,750 | DEVINS ET AL. | |
| | Examiner | Art Unit | |
| | Ayal I. Sharon | 2123 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *26 June 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *2 and 8-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2 and 8-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *4/15/02* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Introduction*

1. Claims 2 and 8-34 of U.S. Application 10/060,750, originally filed on 01/30/2002, are currently pending.
2. The drawing filed on 4/15/02 are accepted.
3. In view of the appeal brief filed on 6/26/2007, PROSECUTION IS HEREBY REOPENED. New grounds of rejection are set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing at the end of the document.

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. The prior art used for these rejections is as follows:

   a. Devins et al., U.S. Patent 6,487,699. ("**Devins**"). Examiner notes that the issued patent has a different inventive entity.

   b. Blaner, B. et al. "An Embedded PowerPC™ SOC for Test and Measurement Applications." 13th Annual IEEE Int'l ASIC/SOC Conf., 2000. Sept. 13-16, 2000. pp.204-208. ("**Blaner**").

7. The claim rejections are hereby summarized for Applicant's convenience. The detailed rejections follow.

**8. Claims 2 and 8-34 rejected under 35 U.S.C. 103(a) as being unpatentable over Devins in view of Blaner.**

9. In regards to Claim 2, Devins teaches the following limitations:

> 2.A verification test bench system for testing a system-on-a-chip (SOC) interface of an SOC, said verification test bench system comprising:
>
> a verification interface model connected to said SOC interface; and

(See Devins: Fig.2, Item 107; and column 4, lines 1-20 and 35-38).

> a test bench external bus interface unit (EBIU) connected to said verification interface model,

(See Devins: Fig.2, Item 202; and column 4, lines 15-20 and 38-40; and col.5, lines 5-8. Item 202 in Figure 2 is expressly labeled as an "External Bus Interface Logic", which examiner interprets as corresponding to the claimed "EBIU").

Moreover, Devins teaches in the summary of the invention that "[a]ccording to the method, an external memory-mapped test device (EMMTD) is coupled between a SOC design being tested in simulation, and cores external to the SOC design." (See Devins: col.2, lines 36-39). Devins further teaches that Fig.2 "shows the internal logic of the EMMTD." (See Devins, col.3, line 3).

While Devins teaches that "External Bus Interface Logic" is used in the EMMTD, Devins does not expressly teach that the same logic (also called "EBIU") is used on the opposite end of the bus, inside the SOC, as claimed in the following claimed limitation (the claim calls it an "SOC EBIU"):

> wherein said test bench EBIU is connected to a SOC EBIU within said SOC, and

Moreover, while Devins teaches that "[a] test case being executed for SOC verification by a simulated embedded processor in the SOC can communicate and control elements external to the SOC, by using the EMMTD to

perform such functions as initiating external core logic ..." (See Devins: col.2, lines 52-57), since Devins does not expressly teach the existence of an SOC EBIU intermediary, Devins only implicitly (not expressly) teaches that the SOC EBIU intermediary "allows" the test case running in said SOC to control both said SOC interface and said verification interface model, as claimed in the following claimed limitations:

> wherein said SOC EBIU allows a test case running in said SOC to control both said SOC interface and said verification interface model.

Blaner, on the other hand, does expressly teach the existence of an SOC EBIU ("External Bus Interface Unit"). Blaner shows an EBIU in the extreme upper-left corner of the SOC block diagram (See Blaner: Fig.2 and p.205). This diagram shows that the SOC EBIU connects externally to "SRAM, Flash, ROM, or an External Master". Examiner interprets the 'External Master' as corresponding to the EMMTD taught in Devins.

Examiner interprets that Blaner's "External Bus Interface Unit", or "EBIU" (See Blaner: p.205) corresponds to Devins' "External Bus Interface Logic" (See Devins: Item 202 in Figure 2). Both are used to interface with an external bus, both operate on opposite ends of that bus, and the difference in the names does not correspond to any real functional difference.

Devins and Blaner are analogous art because they are from the same field of endeavor of System-On-Chip (SOC) testing. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the teachings of Devins with those of Blaner.

The suggestion/motivation for combining the references would have been because Devins teaches a way of controlling SOC tests, while Blaner teaches an SOC in need of testing. More specifically, while Devins teaches that that "External Bus Interface Logic" is used on one end of a bus connecting an SOC to external memory banks, Blaner teaches that the same logic (but relabeled as a "unit", or "EBIU") is used on the opposite end of the same bus.

Therefore, it would have been obvious to a person of ordinary skill in the art to modify Devins with Blaner to obtain the invention as specified in Claims 2.

10. In regards to Claim 8, it is rejected on the same grounds as Claim 2.

> 8.A verification test bench system for testing a system-on-a-chip (SOC) interface of an SOC, said verification test bench system comprising:
>
> a verification interface model connected to said SOC interface; and
>
> a test bench external bus interface unit (EBIU) connected to said verification interface model,
>
> wherein said test bench EBIU is connected to a SOC EBIU within said SOC, and
>
> wherein said test bench EBIU and said SOC EBIU are mastered by the same processor in said SOC.

11. In regards to Claim 9, Blaner teaches the following limitations:

> 9.The verification test bench system in claim 8, wherein said SOC EIBU allows a test case running in said SOC to control both said SOC interface and said verification interface model.

(See Blaner, especially: p.205, "II. SOC Structure" and p.208, "E. Verification Testbench")

Blaner teaches (See "II. SOC Structure". Emphasis added): "... ***The external bus interface unit (EBIU)*** controls up to eight banks of mixed types of memories and operates at one-half the PLB [processor local bus] clock frequency. ... ***Further, the EBIU allows an off-chip device, called the external bus master, to take ownership of the external bus and access attached memories.***"

Blaner also teaches (See "E. Verification Testbench". Emphasis added): "Wrap backs are utilized as much as possible, and behaviorals often contain hard-coded packet or stream data."

Examiner interprets that "Wrap backs" do not containing functioning processors, and therefore must rely on the SOC processor.

12. In regards to Claim 10, Blaner teaches the following limitations:

10. The verification test bench system in claim 8, wherein said SOC interface and said verification interface model are programmed by the same test case running in said SOC.

(See Blaner, especially: p.205, "II. SOC Structure" and p.208, "E. Verification Testbench")

Blaner teaches (See "II. SOC Structure". Emphasis added): "... ***The external bus interface unit (EBIU)*** controls up to eight banks of mixed types of memories and operates at one-half the PLB [processor local bus] clock frequency. ... ***Further, the EBIU allows an off-chip device, called the external bus master, to take ownership of the external bus and access attached memories.***"

Blaner also teaches (See "E. Verification Testbench". Emphasis added): "Wrap backs are utilized as much as possible, and behaviorals often contain hard-coded packet or stream data."

Examiner interprets that "Wrap backs" do not containing functioning processors, and therefore must rely on the SOC processor.

13. In regards to Claim 11, Blaner teaches the following limitations:

11. The verification test bench in claim 11, wherein said test case utilizes the same software driver to configure and control said SOC interface and said verification interface model.

(See Blaner, especially: p.205, "II. SOC Structure")

Blaner teaches (See "II. SOC Structure". Emphasis added): "... ***The external bus interface unit (EBIU)*** controls up to eight banks of mixed types of memories and operates at one-half the PLB [processor local bus] clock frequency. ... ***Further, the EBIU allows an off-chip device, called the external bus master, to take ownership of the external bus and access attached memories.***"

14. In regards to Claim 12, Blaner teaches the following limitations:

12. The verification test bench in claim 11, wherein said test case utilizes different software drivers to configure and control said SOC interface and said verification interface model.

(See Blaner, especially: p.205, "II. SOC Structure")

Blaner teaches (See "II. SOC Structure". Emphasis added): "... ***The external bus interface unit (EBIU) controls up to eight banks of mixed types of memories*** and operates at one-half the PLB [processor local bus] clock frequency. ... Further, the EBIU allows an off-chip device, called the external bus master, to take ownership of the external bus and access attached memories."

15. In regards to Claim 13, Blaner teaches the following limitations:

13. The verification test bench system in claim 8, wherein said verification interface model tests an operational capability of said SOC interface.

(2) Blaner teaches (See "E. Verification Testbench"): "System verification requires stimulus/expectation models or devices to be attached to the external interfaces of the chip. Such models are often implemented in a testbench."

16. In regards to Claim 14, Blaner teaches the following limitations:

14. The verification test bench system in claim 8, further comprising at least one additional verification interface model connected to said test bench EBIU for testing additional types of SOC interfaces.

(See Blaner, especially: p.205, "II. SOC Structure")

Blaner teaches (See "II. SOC Structure". Emphasis added): "... ***The external bus interface unit (EBIU)*** controls up to eight banks of mixed types of memories and operates at one-half the PLB [processor local bus] clock frequency. ... ***Further, the EBIU allows an off-chip device, called the external bus master, to take ownership of the external bus and access attached memories.***"

17. In regards to Claim 15, it is rejected on the same grounds as Claim 2.

15. A verification test bench system for testing a system-on-a-chip (SOC) interface of an SOC, said verification test bench system comprising:

a verification interface model connected to said SOC interface; and

a test bench external bus interface unit (EBIU) connected to said verification interface model,

wherein said test bench EBIU is connected to a SOC EBIU within said SOC, and

wherein said test bench EBIU and said SOC EBIU are mastered by the same processor in said SOC, such that said SOC interface and said verification interface model are programmed by the same test case running in said SOC.

18. In regards to Claim 21, it is rejected on the same grounds as Claim 2.

21.A method of testing a system-on-a-chip (SOC) interface of an SOC, said method comprising:

connecting a verification interface model to said SOC interface;

connecting a test bench external bus interface unit (EBIU) to said verification interface model;

connecting said test bench EBIU to a SOC EBIU within said SOC; and

comparing said SOC interface with said interface model.

19. In regards to Claim 28, Blaner teaches the following limitations:

28.A program storage device readable by machine tangibly embodying a program of instructions executable by the machine to perform a method for testing a system-on-a-chip (SOC)
interface of an SOC, said method comprising:

connecting a verification interface model to said SOC interface;

(See Devins: Fig.2, Item 107; and column 4, lines 1-20 and 35-38).

connecting a test bench external bus interface unit (EBIU) to said verification interface model;

(See Devins: Fig.2, Item 202; and column 4, lines 15-20 and 38-40; and col.5, lines 5-8).

Devins, however, does not expressly teach the following claimed limitations:

connecting said test bench EBIU to a SOC EBIU within said SOC; and

comparing said SOC interface with said interface model.

Blaner, on the other hand, does expressly teach these limitations. Fig.2 of Blaner (see Blaner: p.205), shows an EBIU in the extreme upper-left corner of the SOC block diagram. This diagram shows that the SOC EBIU connects externally to "SRAM, Flash, ROM, or an External Master". Examiner interprets the 'External Master' as corresponding to the EMMTD taught in Devins.

Moreover, Devins also teaches that "A test case being executed for SOC verification by a simulated embedded processor in the SOC can communicate and control elements external to the SOC, by using the EMMTD to perform such functions as initiating external core logic ..." (See Devins: col.2, lines 52-57).

Devins and Blaner are analogous art because they are from the same field of endeavor of System-On-Chip (SOC) testing.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the teachings of Devins with those of Blaner.

The suggestion/motivation for combining the references would have been because Devins teaches a way of controlling SOC tests, while Blaner teaches an SOC in need of testing.

Therefore, it would have been obvious to a person of ordinary skill in the art to modify Devins with Blaner to obtain the invention as specified in Claims 2.

20. Dependent Claims 9, 16, 22, and 29 differ only in the limitations that they inherit from their parent claims. Therefore Claims 16, 22, and 29 are rejected for the same reasons as claim 9, in combination with the rejections of their respective parent claims, which are recited above.

21. Dependent Claims 10, 23, and 30 differ only in the limitations that they inherit from their parent claims. Therefore Claims 23, and 30 are rejected for the same reasons as claim 10, in combination with the rejections of their respective parent claims, which are recited above.

22. Dependent Claims 11, 17, 24, and 31 differ only in the limitations that they inherit from their parent claims. Therefore Claims 17, 24, and 31 are rejected for the same reasons as claim 11, in combination with the rejections of their respective parent claims, which are recited above.

23. Dependent Claims 12, 18, 25, and 32 differ only in the limitations that they inherit from their parent claims. Therefore Claims 18, 25, and 32 are rejected for the same reasons as claim 12, in combination with the rejections of their respective parent claims, which are recited above.

24. Dependent Claims 13, 19, 26, and 33 differ only in the limitations that they inherit from their parent claims. Therefore Claims 19, 26, and 33 are rejected for the same reasons as claim 13, in combination with the rejections of their respective parent claims, which are recited above.

25. Dependent Claims 14, 20, 27, and 34 differ only in the limitations that they inherit from their parent claims. Therefore Claims 20, 27, and 34 are rejected for the same reasons as claim 14, in combination with the rejections of their respective parent claims, which are recited above.

***Response to Arguments***

26. Previously, the Examiner applied separate 35 U.S.C. 102 rejections based on the Devins and Blaner references. The new 35 U.S.C. 103 rejections combine the teachings of the two references.

27. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

***Correspondence Information***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ayal I. Sharon whose telephone number is (571) 272-3714. The examiner can normally be reached on Monday through Thursday, and the first Friday of a biweek, 8:30 am – 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard can be reached at (571) 272-3749.

Any response to this office action should be faxed to (571) 273- 8300, or mailed to:

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Tech Center 2100 Receptionist, whose telephone number is (571) 272-2100.

Ayal I. Sharon
Art Unit 2123
October 14, 2007

PAUL RODRIGUEZ
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100